Phase I Project Summary

Firm: Tech-X Corporation
Contract Number: NNX10CD78P
Project Title: Software Tools for Rapid Algorithm Development on HPC, Data-processing Hardware

Identification and Significance of Innovation: (Limit 200 words or 2,000 characters whichever is less)

Current and future NASA missions are confronted with the challenge that the amount of data collected by its sensors significantly outpaces the down-link bandwidth. As a consequence, initial data reduction has to occur on-board, using algorithms sophisticated enough to sufficiently reduce the amount of data while simultaneously ensuring the preservation of valuable information. This requires enhanced processing power on-board the spacecraft/device/telescope. While future generations of rugged, radiation-hardened hardware can be expected to deliver the necessary performance by employing highly heterogeneous architectures consisting of a combination of FPGAs, DSPs and massively multicore architectures, software development for such devices poses a significant challenge. We propose to develop tools that facilitate and accelerate algorithm development on these hardware devices. The tools will enable scientists to prototype algorithms in the High-Level language that they are most familiar with while simultaneously building code for high-performance computational hardware.

Technical Objectives and Work Plan: (Limit 200 words or 2,000 characters whichever is less)

Objective 1: *Demonstrate the ability to dynamically generate C-code from Octave scripts.*
Objective 2: *Demonstrate the ability to call VSIPL routines in the C-code from overloaded Octave functions.*
Objective 3: *Demonstrate the ability to run advanced data processing algorithms on various accelerator technologies from Octave scripts.*

Task 1: *Modify Octave to Dynamically Generate Compiled C-code*
In this task, we will modify the Octave interpreter to dynamically generate C-code from Octave scripts. This task is in direct support of Objective 1.
Task 2: *Create a Library to Help with Variable Scoping, Allocation and Deletion*
In this task, we will construct a prototype C++ library that will assist our code generation by correctly handling variable declaration, deletion, and scoping in the generated c-code. This task is in support of Objective 1.
Task 3: *Overload Octave Functions to Call Corresponding VSIPL Routines*
In this task, we will overload core Octave computation functions with corresponding VSIPL calls on accelerator technology. This task is in support of Objective 2.
Task 4: *Implement an Accelerated Cloud Detection Algorithm in Octave Script.*
In *this task, we will use the tools developed in tasks 1-3 to implement an accelerated Cloud detection algorithm that runs on FPGAs and GPUs. This task is in support of Objective 3.*

Technical Accomplishments: (Limit 200 words or 2,000 characters whichever is less)

During this phase I SBIR project, we have successfully built the necessary infrastructure for writing and generating code to run on FPGAs, GPUs, or traditional CPUs. The beauty of this development is that one can choose a particular architecture by simply flipping a switch, i.e. the mode in an initialization function. For the FPGA, we have demonstrated a workflow that will allow users of this library to use FPGAs transparently without having to deal with the gory details of (1) bitstream generation from FPGA vendor tools such as ISE from Xilinx and (2) Host-Device Data transfer software. We have also shown that advanced data processing scripts, such as cloud detection, can be executed on GPU hardware through our

library. A full completion of the FPGA code generation aspect, during a phase II of this project, will allow these scripts to be run on FPGAs as well. Moreover, the infrastructure built during phase I will allow the construction of far more advanced, high-performance computational FPGA kernels in phase II.

In summary, we believe our tool could truly allow for rapid advanced FPGA algorithm prototyping if given the funding. Follow-on projects past the phase II would allow us to build Matlab abstractions for more advanced concepts such as using FPGA embedded processors. In addition, there is also potential for adding support for other products such as Handel-C, a competing product to Impulse-C. Handel-C is a widely used for FPGA financial data analysis algorithms.

NASA Application(s): (Limit 100 words or 1,000 characters whichever is less)

The software tools in this project can benefit a variety of current NASA missions including the Landsat Continuity Mission (LDCM), or planned missions like HyspIRI, the hyperspectral infrared imager, ACE, LIST, GEO-CAPE, and DESDynl. These missions offer a glimpse of the flood of data that is going to be expected from far-future missions. This is not only a challenge encountered with Earth Science missions, but with all future missions, including the Solar Dynamics Observatory or the James Webb Space Telescope. Mechanisms currently used or investigated to reduce the amount of data prior to transmission to Earth ranges from fairly simple trigger functions as encountered on board of RHESSI or planned for XMM, to more complex cloud detector algorithms on board the Earth Observing System (EOS) mission.

Non-NASA Commercial Application(s): (Limit 200 words or 2,000 characters whichever is less)

Modern computational accelerator technologies like FPGAs and GPUs can be difficult to program efficiently and effectively due to the complex nature of the underlying hardware. Many companies provide libraries with highly specialized algorithms that can be accessed from compiled languages like C/C++/Fortran. However, this presents another barrier for many scientists who generally program in high-level languages like MATLAB and IDL. The tools developed in this project, can make these computational accelerators easily accessible to a much wider range of scientists through open source high level languages.

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